25. (New) The apparatus of Claim 24, the first source register address and the second source-destination register address each consisting of three bits.

26. (New) The apparatus of Claim 24, the first register corresponding to the first source register address.

27. (New) The apparatus of Claim 24, the second register corresponding to the second source-destination register address.

28. (New) The apparatus of Claim 27, the third register corresponding to the second source-destination register address.

29. (New) The apparatus of Claim 24 wherein the decoder further decodes the unpack instruction, a first byte and a second byte of the three bytes comprising an operation code specifying an unpack operation to interleave low order packed elements from the first and second packed data, the elements selected from the group consisting of byte elements, word elements and doubleword elements.

30. (New) The apparatus of Claim 24 further comprising:

a memory to hold the unpack instruction; and

a storage device to hold software, the software configured to supply the unpack instruction to the memory for execution.

31. (New) The apparatus of Claim 30, the instruction decoder to receive and decode the unpack instruction from the memory, the first register corresponding to the first source register address, the second register corresponding to the second source-destination register address.

32. (New) The apparatus of Claim 31, the third register corresponding to the second source-destination register address.

33. (New) The apparatus of Claim 32, the first source register address and the second source-destination register address each consisting of three bits.

34. (New) The apparatus of Claim 15 wherein each of the first packed data element, the second packed data element, the third packed data element, and the fourth packed data element has a length of N/2 bits; and the circuit is coupled to the decoder to unpack the first packed data and the second packed data to produce an unpacked data element having a length of N bits in response to the unpack instruction, said unpacked data element comprising the first packed data element but not the third packed data element of the first packed data, and the second packed data element but not the fourth packed data element of the second packed data.

35. (New) The apparatus of Claim 34 wherein the first packed data element is a low order data element of the first packed data and the second packed data element is a low order data element of the second packed data and the unpack instruction comprises an opcode field to contain one of a set of operation codes to specify an unpack operation interleaving low order data elements from the first and the second pluralities of data elements, the opcode field specifying data elements selected from the group consisting of byte elements, word elements and doubleword elements.

36. (New) The apparatus of Claim 35 wherein the opcode field of the unpack instruction contains one of a set of operation codes comprising the hexadecimal values 0F60, 0F61 and 0F62.